Test Design for Computer Systems with Life-Time Perspective Project 05.06

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1 Summary

While it is possible to manufacture integrated circuits (ICs) with billions of transistors that are squeezed on dies sized a few square millimeters, it is a major challenge to ensure that all transistors in the final IC are fault-free. ICs can become defective already at manufacturing or become defective while in operation. It is obvious that defective ICs are to be avoided as they may impose much harm. A failing IC can make the whole system fail.

There are two communities that address defective ICs. The manufacturing community that addresses manufacturing test of ICs and the fault-tolerance community that addresses defects in a system while in operation. Two communities leads to separate solutions, that is costly, ineffective and lead to suboptimal solutions. The aim of this project is to include manufacturing test problems and fault-tolerance problems in one framework and address the problems with a life-time perspective. The objective of the project is to find schemes that can be used from manufacturing and throughout the life-time of a system to test, diagnose and adjust the system such that it behaves as error-free even when there are errors in the system.

The main achievements of the project are:

- the Institution of Engineering and Technology (IET) Premium Award (2009) for a novel architecture to be used at manufacturing test.
- a paper included in Design, Automation, and Test in Europe, The Most Influential Papers of 10 Years DATE, and 3 papers were best paper candidates (DATE, ETS and WRTLT)
- one thesis received *Lilla Polhemspriset* - Best Master thesis in Sweden and one thesis was selected as best thesis at the Department of Computer and Information Science
- an in-house CAD-tool used at NXP Semiconductors for scan-chain diagnosis
- 1 docent (Erik Larsson), 1 Ph.D thesis (Anders Larsson), 1 Licentiate thesis (Anders Larsson), and 30 Master/Bachelor theses
- 75 publications which are distributed as 1 book, 5 book chapters, 8 journal papers, 31 conference papers, and 30 workshop papers
- collaboration with Ericsson (Sweden), SAAB (Sweden), Philips Research (The Netherlands), NXP Semiconductors (The Netherlands), Duke University (USA), Indian Institute of Science (India), University of Bologna (Italy), and FP7 partners: Tallinn Technical University, Bremen University, Graz University, Ericsson (Sweden), IBM (Israel), Testonica (Estonia) and TransEDA (UK)

- Erik Larsson made a Stiftelsen for Strategisk Forskning (SSF) supported sabbatical visit (12 months) at NXP Semiconductors, Eindhoven, The Netherlands, and Anders Larsson made a 3-month research visit at Duke University, USA
- a joint Ph.D. course with Jerzy Dabrowski (project 03.03 - Testability-Oriented Design Techniques for Mixed-Signal/RF Integrated Circuits)
- funding from FP7 (Specific Targeted Research Projects (STREP) DIAMOND - Diagnosis, Error Modelling and Correction for Reliable Systems Design), Swedish Research Council (Vetenskapsrådet (VR)), Stiftelsen for Strategisk Forskning (SSF), Stiftelsen for internationalisering av högre utbildning och forskning (STINT), Ericsson
- the creation of a research group currently consisting of one post doc and three Ph.D. students

The CENIIT funding has been a key component to enable the reception of external funding. The CENIIT funding has partially supported Erik Larsson (project leader), Anders Larsson (Ph.D. students (graduated 2008)), Dimitar Nikolov (Ph.D. student from 2009) and Urban Ingelsson (Post doc from 2009).

The rest of the report is organized as follows. First awards are detailed, followed by a discussion on collaborations. Then funding is discussed and finally all publications, including Ph.D., Lic, Master/Bachelor theses and research papers are listed.

2 Awards

The following awards have been received.

- The paper *Architecture for Integrated Test Data Compression and Abort-on-Fail Testing in a Multi-Site Environment* by Erik Larsson received the Institution of Engineering and Technology (IET) Premium Award, 2009
- The paper *An Integrated System-on-Chip Test Framework* by Erik Larsson and Zebo Peng has been selected to be included in Design, Automation, and Test in Europe, The Most Influential Papers of 10 Years DATE, 2008
- *Lilla Polhemspriset* - Best Master thesis in Sweden was given to Dan Adolfsson for the thesis *Improved Scan Chain Diagnosis*, 2008
- Best master thesis: Dataföreningen, östra Kretsen in co-operation with the Department of Computer and Information Science at Linköpings Universitet rewarded the Master Thesis by Urban Ingelsson, *Test Scheduling for Modular SOCs in an Abort-on-Fail Environment*, 2005
- The following papers have been best paper candidates:
  - Mikael Väyrynen, Virendra Singh, and Erik Larsson, *Fault-Tolerant Average Execution Time Optimization for General-Purpose Multi-Processor System-on-Chips*, Design Automation and Test in Europe (DATE 2009), pages 484-489, Nice, France, April, 2009

- Urban Ingelsson, Sandeep Goel, Erik Larsson, and Erik Jan Marinissen, *Test Scheduling for Modular SOCs in an Abort-on-Fail Environment*, European Test Symposium (ETS'05), Tallinn, Estonia on May 22-25, 2005, pages 8-13
- *A Test Data Compression Architecture with Abort-on Fail Capability*, Erik Larsson and Irtiyaz Gilani, IEEE Workshop on RTL and High Level Testing (WRTLT), Harbin, China, July 20-21, 2005

3 Collaborations

Below collaborations are detailed.

- Ericsson, Stockholm, Sweden. The collaboration with Gunnar Carlsson focuses on test problems in advanced computer systems, such as telecommunication base stations, at both IC-level and system-level. The collaboration has resulted in a three thesis projects, 10 research papers distributed as 5 conference papers and 5 workshop papers. Currently we collaborate within the FP7 project.
- NXP Semiconductors (previously Philips Research), Eindhoven, The Netherlands. Erik Larsson made invited talks and has spent a sabbatical of 12 month. There has been 3 theses of which one was selected as winner of Lilla Polhems priest (2008) and one thesis was selected as best thesis at the Department of Computer Science (2005). The collaboration has resulted in 5 conference papers and 4 workshop papers.
- SAAB, Stockholm, Sweden. Embedded test solutions have been developed through a joint Master thesis project. SAAB have donated test equipment that is used in education and research.
- Indian Institute of Science, India, Dr Virendra Singh. The collaboration is supported by STINT. The collaboration has generated 20 publications distributed as 1 book chapter, 10 conference papers and 9 workshop papers. Invited talks has been given at Indian Institute of Science. Several research visits have been performed where researchers from Indian Institute of Science have visited LiU and researchers from LiU have visited Indian Institute of Science. The International Workshop on Reliability Aware System Design and Test (RAS-DAT) which is running in conjunction with VLSI Design have been created and organized in january 2010 and 2011 with more than 70 attendees at each occasion.
- Duke University, USA, Professor Krishnendu Chakrabarty. Anders Larsson made a 3-month visit at Duke University. We jointly gave a tutorial at VLSI Design and Test Symposium (VDAT), Kolkata, India, 2007 and produced 1 book chapter, 1 journal paper, 3 conference papers and 1 workshop paper.
- Bologna University, Italy, Professor Cecilia Metra. The collaboration includes an invited talk at University of Bologna and currently a Master thesis student from Bologna University is finalizing his thesis at LiU.
- Ph.D. course with Jerzy Dabrowski (project 03.03 - Testability-Oriented Design Techniques for Mixed-Signal/RF Integrated Circuits). 16 students from different departments at LiU attended the course. The plan is to repeat the course on a regular basis.

4 Sources of Funding and Budget

In this section, we detail the sources of funding, the spending of the funding, including the CENIIT funding.

Erik Larsson is project leader for projects supported from the following sources:

- Center for Industrial Information Technology (CENIIT) project: *Test design for computer systems with a life-time perspective*, 2005-2010
- Scholarship from Ericsson AB, 2007
- Swedish Foundation for Strategic Research (SSF) - Strategisk mobilitet at NXP Semiconductors, Eindhoven, 2008-2010
- The Swedish Foundation for International Cooperation in Research and Higher Education (STINT), Institutional Grant for Younger Researchers for establishing collaborations with Dr. Virendra Singh at Indian Institute of Science, Bangalore, 2008-2011
- Swedish Research Council (Vetenskaprrådet (VR)), Fault-tolerant design and optimization for multi-processor system-on-chip, 2010-2013
- FP7 (ICT-2009-4) - Diagnosis and Model-Based Debug in Embedded Systems Design (DIAMOND), Small or medium-scale focused research project (STREP), 2010-2013

Table 1 details the approximate spendings of CENIIT and other fundings per person in the group. For example, in 2005, Erik Larsson was covered by 40% from CENIIT and 60% from teaching and administration (TA). The approximate report is due to that both project applications often are accepted in an non-deterministic way and do often not match the length of the Ph.D. program. Further, administrative duties may vary over time. Teaching load depends for example on the number of students.

The support from the SSF supported STRINGENT project led by Professor Christer Svensson is acknowledged and appreciated. The STRINGENT funding and the CENITT funding have been key components to form a research group. The current funding is all from external funding agencies.

The external funding covers the group, that is Erik Larsson, Urban Ingenlsson (post doc), Dimitar Nikolov (Ph. D. student), Mudassar Majeed (Ph. D. student), and Breeta Sen Gupta (Ph. D. student).

5 Degrees and Publications

The section summarizes the results in the project. The project has produced 1 Docent (Erik Larsson), 1 Ph.D. (Anders Larsson), 1 Lic. (Anders Larsson) and 30 Master and Bachelor theses. During the project, there has been 17 talks distributed as 14 invited talks, 1 keynote talk, and 2 tutorials. The project has produced 75 publications distributed as 1 book, 5 book chapters, 8 journal papers, 31 conference papers and 30 workshop papers.

Table 1: Approximate spending

	Funding [a]	2005	2006	2007	2008	2009	2010
Erik Larsson	CENIIT	40%	50%	39%	25%	14%	15%
	SSF				25%	50%	25%
	STINT				10%	10%	10%
	FP7						15%
	TA	60%	50%	61%	40%	26%	35%
Anders Larsson [b]	CENIIT	30%	30%	30%	30%		
	STRINGENT [c]	50%	50%	50%	35%		
	TA	20%	20%	20%	10%		
Dimitar Nikolov [d]	CENIIT					55%	5%
	FP7						50%
	STINT					10%	10%
	TA					10%	35%
Urban Ingelsson [e]	CENIIT					25%	30%
	FP7						50%
	STINT						10%
	TA						10%
Mudassar Majeed [f]	HEC						83%
Breeta Sen Gupta [g]	VR						10%
	FP7						52%
	TA						15%

[a] TA-Teaching and administration, SSF - Stiftelsen för strategisk forsaking, STINT - The Swedish Foundation for International Cooperation in Research and Higher Education, VR - Vetenskapsrådet, FP7 - DIAMOND (STREP project), HEC - Higher Education Commission of Pakistan

[b] Ph.D. student until 2008-09-01

[c] The SSF supported STRINGENT project led by Professor Christer Svensson supported Anders Larsson with 50%

[d] Ph.D. student from 2009-04-01

[e] Post doc from 2009-09-01

[f] Ph.D. student from 2010-03-01 with scholarship from HEC

[g] Ph.D. student from 2010-05-01

5.1 Theses

5.1.1 Lic. and Ph.D. theses

1. Anders Larsson, System-on-Chip Test Scheduling and Test Infrastructure Design, Licentiate Thesis No. 1206, Linkping University, November 2005

2. Anders Larsson, Test Optimization for Core-based System-on-Chip, PhD Thesis No. 1222, November 2008 (Erik Larsson main supervisor)

5.1.2 Master and Bachelor theses

1. Farrokh Ghani Zadegan, Analysis and Optimization for Testing Using IEEE P1687, LIU-IDA/LITH-EX-A–10/040–SE

2. Shih-Yen Chang, Placement of measurement points for wear-out prediction with regard to

electromigration, LIU-IDA/LITH-EX-A–10/033–SE

3. Erik Karlsson, Analysis and Development of Error-free Job Mappping and Scheduling for Network-on-Chips with Homogenous Processors, LIU-IDA/LITH-EX-G–10/007–SE

4. Daniel Ahlström, Minimizing memory requirements for deterministic test data in embedded testing, LIU-IDA/LITH-EX-G–10/006–SE

5. Niklas Huss, Automating IEEE 1500 Wrapper Insertion, LIU-IDA/LITH-EX-A–09/055–SE

6. Aijaz Baig, Embedded Boundary Scan for Test and Debug, LIU-IDA/LITH-EX-A–09/031–SE

7. Mikael Väyrynen, Fault-Tolerant Average Execution Time Optimization for General-Purpose Multi-Processor System-on-Chips, LIU-IDA/LITH-EX-A–09/022–SE

8. Boris Asadanin, Optimizing Mobile Phone Free Fall Drop Test Equipment - Precision, Repeatability, and Time Efficiency LIU-IDA/LITH-EX-A–08/060–SE

9. Joanna Siew, Advanced Scan Chain Diagnosis Algorithms. LITH-IDA/LITH-EX-A–08/027–SE

10. Stefan Trimmel, Utvärdering av modellbaserad testning av en basstationskontroller. LITH-IDA/LITH-EX-A–08/023–SE

11. Michael Söderman, Loss-less on-chip test response compression for diagnosis and debug in volume production of system-on-chip. LITH-IDA/LITH-EX-A–08/009–SE

12. Niklas Brammer, Undersökning av automatiserad interoperabilitetstest av mobila terminaler. LITH-IDA/LITH-EX-A–08/009–SE

13. Xin Zhang, Core-level compression technique selection and SOC test architecture co-optimization. LITH-IDA/LITH-EX-A–08/003–SE

14. Dan Adolfsson Improved Scan Chain Diagnosis. LITH-IDA/DS-EX–07/005–SE

15. Mikael Löfqvist, Open Code Translation from Executable and Translatable UML Models - Implicit Bridging. LITH-IDA/DS-EX–07/004–SE

16. Katarina Larsson, Komprimering av testdata för SOC - En implementation av metoden vector repeat. LITH-IDA/DS-EX-ING–07/002–SE

17. Tobias Dubois, Test Quality Analysis and Improvement for an Embedded Asynchronous FIFO. LITH-IDA/DS-EX–07/002–SE

18. Fredrik Andersson Utvärdering av Project Blackdog, LITH-IDA/DS-EX-ING–07/001–SE

19. Johan Holmqvist, Utvärdering och vidareutveckling av STAPL för användning inom inbäddad Boundary-Scan baserad test. LITH-IDA/DS-EX–07/001–SE

20. Karl Andersson SoC Test Data Compression in an Abort-on-fail Environment. LITH-IDA/DS-EX–06/010–SE

21. Karin Hedlund, Multi-site SOC Test with Replace-on-fail and Module Configuration. LITH-IDA/DS-EX–06/003–SE

22. Thomas Jansson, Core-based System-on-Chip Test Scheduling with Process Variations. LITH-IDA/DS-EX-ING–06/001–SE

23. Mikko Selkälä , Test Data Analysis for Accurate Power Estimation. LITH-IDA/DS-EX–06/004–SE

24. Per Beijer, Testkostnadsminimering för system p kisel genom integrerat val av test, schemaläggning och TAM-design. LITH-IDA/DS-EX-ING–05/003–SE

25. David Bäckström, Boundary-Scan in the ATCA standard. LITH-IDA/DS-EX–05/008–SE

26. Soheil Samii, Power Modeling and Scheduling of Tests for Core-based System Chips. LITH-IDA/DS-EX–05/006–SE

27. Jon Persson, Deterministic Test Vector Compression/Decompression Using an Embedded Processor and Facsimile Coding. LITH-IDA/DS-EX–05/033–SE

28. Erik Stenlund & Tobias Palmkvist, Design och implementation av en röststyrd mobil robot. LITH-IDA/DS-EX-ING–05/002–SE

29. Aksel Willgert & Andreas Viitanen, Exploring the impact of Power Modeling Accuracy in System-on-Chip Design Flow. LITH-IDA/DS-EX-ING–05/001–SE

30. Urban Ingelsson, Test scheduling for embedded-core based SoCs in an abort-on-fail environment. LITH-IDA/DS-EX–05/001–SE

5.2 Invited Talks, Keynote Talks, and Tutorials

1. Erik Larsson, Testing advanced electronics systems (Tutorial), IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Malaysia, December 2010

2. Erik Larsson, A Distributed Architecture for Checking Global Properties during Post Silicon Debug (Elevator talk), International Test Conference (ITC), Austin, Texas, USA, November 2009

3. Erik Larsson, Checking distributed properties during post silicon debug (Invited talk), Tallinn Technical University, Tallinn, Estonia, February 2010

4. Erik Larsson, Throughput and Diagnosis - Co-Maximization (Elevator talk), International Test Conference (ITC), Austin, Texas, USA, November 2009

5. Erik Larsson, Fault-Tolerant Average Execution Time Optimization for General-Purpose Multi-Processor System-on-Chip (Invited talk), Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium, May 2009

6. Erik Larsson, Power-Aware SOC Test Planning (Keynote), Workshop on RTL and High Level Testing (WRTLT), Sapporo, Japan, November 2008

7. Erik Larsson, Improved Scan-Chain Diagnosis (Invited talk), SAAB, Linköping, Sweden, May 2008

8. Erik Larsson, An X-Tolerant and Diagnostic Friendly Approach to Integrate Abort-on-Fail Test and Test Data Compression in a Multi-site Environment (Invited talk), University of Bologna, Bologna, Italy, May 2008

9. Erik Larsson, Power-Constrained Test Design for Modular System-on-Chip (Invited talk), Indian Institute of Science, Bangalore, India, January 2008

10. Erik Larsson, An X-Tolerant and Diagnostic Friendly Approach to Integrate Abort-on-Fail Test and Test Data Compression in a Multi-site Environment (Invited talk), Synopsis, San Jose, CA, USA, October 2007

11. Erik Larsson, Testing System Chips (Invited talk), NXP Semiconductors - Corporate Innovation Technology, Eindhoven, The Netherlands, September 2007

12. Erik Larsson, Testing System Chips (Invited talk), Indian Institute of Science, Bangalore, India, August 2007

13. Erik Larsson and Krishnendu Chakrabarty (Tutorial), Manufacturing Test Solutions for System-On-Chip Integrated Circuits, VLSI Design and Test Symposium (VDAT), Kolkata, India, August 2007

14. Erik Larsson, Testing System Chips (Invited talk), The Chinese University of Hong Kong, Hong Kong, China, January 2007

15. Erik Larsson, Testing System Chips (Invited talk), Nara Institute of Science and Technology, Nara, Japan,January 2007

16. Erik Larsson, Test Preparation and Application for System Chips (Invited talk), Tallinn Technical University, Tallinn, Estonia, September 2006

17. Erik Larsson, Test Preparation and Application for System Chips (Invited talk), Universität Potsdam, Potsdam, Germany, May 2006

5.3 Scientific publications

5.3.1 Books and book chapters

1. Dimitar Nikolov, Mikael Väyrynen, Urban Ingelsson, Erik Larsson, and Virendra Singh, Optimizing Fault Tolerance for Multi-Processor System-on-Chip, Design and Test Technology for Dependable Systems-on-chip, Raimund Ubar, Jaan Raik, Heinrich Theodor Vierhaus (Eds.), 2010, Hardcover, ISBN: 978-1-6096-0212-3

2. Anders Larsson, Urban Ingelsson, Erik Larsson, and Krishnendu Chakrabarty, Study on Combined Test-Data Compression and Test Planning for Testing of Modular SoCs, Design and Test Technology for Dependable Systems-on-chip, Raimund Ubar, Jaan Raik, Heinrich Theodor Vierhaus (Eds.), 2010, Hardcover, ISBN: 978-1-6096-0212-3

3. Erik Larsson and C.P. Ravikumar, Power-Aware System-Level DfT and Test Planning, Power-Aware Testing and Test Strategies for Low Power Devices, Patrick Girard, Nicola Nicolici, Xiaoqing Wen (Eds.), 2009, Approx. 400 p. 222 illus., Hardcover ISBN: 978-1-4419-0927-5

4. Erik Larsson and Zebo Peng, An Integrated System-on-Chip Test Framework, Design, Automation, and Test in Europe, The Most Influential Papers of 10 Years DATE, Lauwereins, Rudy; Madsen, Jan (Eds.), 2008, pages 439-454, Hardcover, ISBN: 978-1-4020-6487-6

5. Erik Larsson and Stina Edbom, Combined Test Data Selection and Scheduling for Test Quality Optimization under ATE Memory Depth Constraint, Vlsi-Soc: From Systems To Silicon, pages 221-244, ISBN: 978-0-387-73660-0, DOI: 10.1007/978-0-387-73661-7, October 2007

6. Erik Larsson, Introduction to Advanced System-on-Chip Test Design and Optimization , FRONTIERS IN ELECTRONIC TESTING : Volume 29,,Springer, ISBN: 1-4020-3207-2, May 2005

5.3.2 Journal papers

1. Erik Larsson, Architecture for Integrated Test Data Compression and Abort-on-Fail Testing in a Multi-Site Environment , IET Computers & Digital Techniques, July 2008, Volume 2, Issue 4 pages 275-284

2. Erik Larsson and Zebo Peng, A Reconfigurable Power Conscious Core Wrapper and its Application to System-on-Chip Test Scheduling , Journal of Electronic Testing: Theory and Application, ISSN 0923-8174 (Print), 1573-0727 (Online), DOI 10.1007/s10836-008-5074-2

3. Soheil Samii, Mikko Selkälä, Erik Larsson, Krishnendu Chakrabarty, and Zebo Peng, Cycle-Accurate Test Power Modeling and its Application to SoC Test Architecture Design and Scheduling, IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977, Digital Object Identifier 10.1109/TCAD.2008.917974

4. Erik Larsson and Stina Edbom, Test Data Truncation for Test Quality Maximization under ATE Memory Depth Constraint IET Computers & Digital Techniques, Volume 1, Issue 1, January 2007, pages 27-37, ISSN: 1751-861X, (Digital Object Identifier: 10.1049/iet-cdt:20050209)

5. Erik Larsson and Hideo Fujiwara, System-on-Chip Test Scheduling with Reconfigurable Core Wrappers, Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 3, March 2006, pages 305-309, ISSN: 1063-8210, (Digital Object Identifier: 10.1109/TVLSI.2006.871757)

6. Erik Larsson and Zebo Peng, Power-Aware Test Planning in the Early System-On-Chip Design Exploration Process, Transactions on Computers, Volume 55, Number 2, February 2006, pages 227-239, ISSN: 0018-9340, Digital Object Identifier: 10.1109/TC.2006.28

7. Erik Larsson, Julien Pouget, and Zebo Peng, Abort-on-Fail Based Test Scheduling, Journal of Electronic Testing; Theory and Applications (JETTA), Volume 21, Number 6, December 2005, pages 651 - 658, ISSN 0923-8174 (Print) 1573-0727 (Online), Digital Object Identifier: 10.1007/s10836-005-4597-z

8. Julien Pouget, Erik Larsson, and Zebo Peng, Multiple Constraints Driven System-on-Chip Test Time Optimization, Journal of Electronic Testing; Theory and Applications (JETTA), Volume 21, Number 6, December 2005, pages 599-611, ISSN 0923-8174 (Print) 1573-0727 (Online), Digital Object Identifier: 10.1007/s10836-005-2911-4

5.3.3 Conference papers

1. Farrokh Ghani Zadegan, Urban Ingelsson, Gunnar Carlsson and Erik Larsson Design Automation for IEEE P1687, Design Automation and Test in Europe (DATE011), Grenoble, France, March 2011

2. Breeta SenGupta, Urban Ingelsson and Erik Larsson, Scheduling Tests for 3D Stacked Chips under Power Constraints, The 6th International Symposium on Electronic Design, Test and Applications (DELTA 2011), Queenstown, New Zealand, January 2011

3. Vinay N.S., Indira Rawat, M.S. Gaur, Erik Larsson,and Virendra Singh, Thermal Aware Test Scheduling for Stacked Multi-Chip-Modules, IEEE EAST-WEST DESIGN & TEST SYMPOSIUM (EWDTS), St. Petersburg, Russia, September 17-20, 2010

4. Farrokh Ghani Zadegan, Urban Ingelsson, Gunnar Carlsson and Erik Larsson Test Time Analysis for IEEE P1687, IEEE 19th Asian Test Symposium(ATS2010), Shanghai, China, December 2010

5. Mudassar Majeed, Daniel Ahlström, Urban Ingelsson, Gunnar Carlsson and Erik Larsson, Efficient embedding of deterministic test data, IEEE 19th Asian Test Symposium(ATS2010), Shanghai, China, December 2010

6. Pramod Subramanyan, Virendra Singh, Kewal Saluja, and Erik Larsson, Energy-Efficient Fault Tolerance in Chip Multiprocessors Using Critical Value Forwarding, The 40th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Fairmont Chicago, Millennium Park, Chicago, Illinois, USA, June 28-July 1, 2010, pages 121-130

7. Erik Larsson, Bart Vermeulen, and Kees Goossens, A Distributed Architecture to Check Global Properties for Post-Silicon Debug, IEEE European Test Symposium (ETS), Prague, Czech Republic, May 2010, pp. 182-187

8. Jaynarayan Tudu, Erik Larsson, Virendra Singh, and Hideo Fujiwara, Scan Cells Reordering to Minimize Peak Power During Test Cycle: A Graph Theoretic Approach, IEEE European Test Symposium (ETS), Prague, Czech Republic, May 2010, pages 182-187

9. Pramod Subramanyan, Virendra Singh, Kewal Saluja and Erik Larsson, Energy-Efficient Redundant Execution for Chip Multiprocessors Great Lakes Symposium on VLSI on (GLSVLSI), Rhode Island, USA, May 2010

10. Jaynarayan Tudu, Erik Larsson, Virendra Singh, and Hideo Fujiwara, Graph Theoretic Approach for Scan Cell Reordering to Minimize Peak Shift Power Great Lakes Symposium on VLSI on (GLSVLSI), Rhode Island, USA, May 2010

11. Pramod Subramanyan, Virendra Singh, Kewal K. Saluja and Erik Larsson, Multiplexed Redundant Execution: A Technique for Efficient Fault Tolerance in Chip Multiprocessors, Design Automation and Test in Europe (DATE), Dresden, Germany, March 2010

12. Dimitar Nikolov, Urban Ingelsson, Virendra Singh and Erik Larsson, Estimating Error-probability and its Application for Optimizing Roll-back Recovery with Checkpointing, IEEE International Symposium on Electronic Design, Test & Applications (DELTA), Ho Chi Minh City, Vietnam, January, 2010

13. Dan Adolfsson, Joanna Siew, Erik Jan Marinissen, Erik Larsson, On Scan Chain Diagnosis for Intermittent Faults, IEEE Asian Test Symposium (ATS), Taichung, Taiwan, November, 2009, pages 47-54

14. Jaynarayan T Tudu, Erik Larsson, Virendra Singh, and Adit Singh, Capture Power Reduction for Modular System-on-Chip Test, IEEE/VSI VLSI Design and Test Symposium (VDAT), Bangalore, India, July, 2009

15. Jaynarayan T Tudu, Erik Larsson, Virendra Singh, and Vishwani Agrawal, On minimization of peak power for scan circuit during test, European Test Symposium (ETS 2009), pages 25-30, Sevilla, Spain, May, 2009

16. Mikael Väyrynen, Virendra Singh, and Erik Larsson, Fault-Tolerant Average Execution Time Optimization for General-Purpose Multi-Processor System-on-Chips, Design Automation and Test in Europe (DATE 2009), pages 484-489, Nice, France, April, 2009

17. Anders Larsson, Xin Zhang, Erik Larsson, and Krishnendu Chakrabarty, Core-Level Expansion of Compressed Test Patterns, Asian Test Symposium (ATS 2008), Sapporo, Japan, November 24-27, 2008

18. Anders Larsson, Erik Larsson, Krishnendu Chakrabarty, Petru Eles, and Zebo Peng, Test-Architecture Optimization and Test Scheduling for SOCs with Core-Level Expansion of Compressed Test Patterns, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, pages 188-193, March 10-14, 2008

19. Gunnar Carlsson, Johan Holmqvist, Erik Larsson, Protocol Requirements in an SJTAG/IJTAG Environment, International Test Conference (ITC'07) Santa Clara, CA, USA, October 2007, Lecture 1.3

20. Erik Larsson, Mehdi Amirijoo, Daniel Karlsson, Petru Eles, What impacts course evaluation?, 12th Annual Conference on Innovation and Technology in Computer Science Education, Dundee, Scotland, June 25-27, 2007, page 333, ISSN:0097-8418

21. Tobias Dubois, Mohamed Azimane, Erik Larsson, Erik Jan Marinissen, Paul Wielage and Clemens Wouters, Test Quality Analysis and Improvement for an Embedded Asynchronous FIFO, Design, Automation, and Test in Europe Conference (DATE'07) Nice, France April 2007, pages 859-864, ISBN:978-3-9810801-2-4, Digital Object Identifier: 10.1145/1266366.1266552

22. Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, Optimized Integration of Test Compression and Sharing for SOC Testing, Design, Automation, and Test in Europe Conference (DATE'07) Nice, France, April 2007, pages 207-212, ISBN: 978-3-9810801-2-4, Digital Object Identifier: 10.1109/DATE.2007.364592

23. Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, A Heuristic for Concurrent SOC Test Scheduling with Compression and Sharing, IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS'07) Krakow, Poland, April 2007, pages 61-66

24. Erik Larsson and Jon Persson, An Architecture for Combined Test Data Compression and Abort-on-Fail Test, Asia and South Pacific Design Automation Conference (ASP-DAC'07), Yokohama, Japan, January 23-26, 2007, pages 726-731, ISBN: 1-4244-0630-7, Digital Object Identifier: 10.1109/ASPDAC.2007.358073

25. Erik Larsson, Combined Test Data Compression and Abort-on-Fail Testing, 24th Norchip Conference, Linkoping, Sweden, November 20-21, 2006, pages 137-140, Digital Object Identifier: 10.1109/NORCHP.2006.329262

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